S/N 09/739,589

Docket No.: SPLX.P014

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

Express Mail Label No.: EL714233295US Date of Deposit: December 15, 2000

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Mark Adeli

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Steven Teig, et al.

Serial No.: Not Yet Assigned

Filed: Herewith

For: **Method and Apparatus for Pre-Computing and Using Multiple Placement Cost Attributes to Quantify the Quality of a Placement Configuration within a Partitioned Region**

PRELIMINARY AMENDMENT

Box PATENT APPLICATION
Assistant Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Sir:

This Preliminary Amendment is concurrently filed with the above-entitled application, which is a continuation application of a presently pending application entitled "Recursive Partitioning Placement Method and Apparatus," filed on December 6, 2000.

Applicants respectfully request that claims 1-27 be canceled (pursuant to the amendment below) before calculation of the filing fee.

IN THE TITLE

Please replace the current title, "Recursive Partitioning Placement Method and Apparatus," with "Method and Apparatus for Pre-Computing and Using Multiple Placement Cost Attributes to Quantify the Quality of a Placement Configuration within a Partitioned Region."

IN THE SPECIFICATION

On page 1, line 1, please delete "The invention is directed towards recursive partitioning placement method and apparatus" and insert--

Cross Reference to Related Applications

This application is a continuation application of United States Patent Application entitled "Recursive Partitioning Placement Method and Apparatus," filed on December 6, 2000, and having the Serial No. _____.

Field of the Invention

The invention is directed towards method and apparatus for pre-computing and using multiple placement cost attributes to quantify the quality of a placement configuration within a partitioned region.--

IN THE CLAIMS

Please cancel claims 1-27, and add the following new claims.

28. (New) For a placer that places circuit modules in integrated-circuit ("IC") layouts, the placer using a set of partitioning lines, that define a plurality of slots, to partition an IC layout region into a plurality of sub-regions corresponding to said slots, a method of pre-computing costs of placing circuit modules in an IC-layout region, the method comprising:

a) selecting a first group of said slots;

b) computing a first attribute of a set of one or more interconnect lines necessary for connecting the first group of said slots;

c) computing a second attribute of the set of interconnect lines;

d) storing the computed attributes in a storage structure.

29. (New) The method of claim 28 wherein computing the first attribute comprises calculating the length of said set of interconnect lines.

30. (New) The method of claim 28 wherein computing the second attribute comprises calculating number of bends in said set of interconnect lines.

31. (New) The method of claim 30 wherein the bends are diagonal bends.

32. (New) The method of claim 28, wherein a plurality of line paths exist between said slots, wherein computing the first attribute comprises identifying the line paths used by said set of interconnect lines.

33. (New) The method of claim 28, wherein a plurality of edges exist between said slots, wherein computing the first attribute comprises identifying the edges intersected by said set of interconnect lines.

34. (New) The method of claim 28 further comprising:

a) computing a third attribute of the set of interconnect lines; and

b) storing the computed third attributes in the storage structure.

35. (New) The method of claim 28 further comprising:

a) selecting a second group of said slots different from said first group;

b) computing first and second attributes of a set of one or more interconnect lines connecting the second group of said slots;

c) storing the computed attributes in the storage structure.

36. (New) For an electronic design automation ("EDA") application that performs placement operations, a method of pre-computing costs of placing circuit elements within an integrated-circuit ("IC") layout, the method comprising:

a) defining a partitioning grid having a plurality of slots, said partitioning grid for partitioning a region of an IC layout during a placement operation;

b) for each combination of said slots, defining at least one connection graph that models the topology of interconnect lines necessary for connecting the combination of said slots;

c) computing multiple attributes for each of said connection graphs;

d) storing the computed attributes in a storage structure.

37. (New) The method of claim 36, wherein the connection graphs are Steiner trees.

38. (New) The method of claim 36, wherein the connection graphs are minimum spanning trees.

39. (New) The method of claim 36, wherein computing multiple attributes of each connection graph comprises calculating the length of each graph.

40. (New) The method of claim 36, wherein computing multiple attributes of each connection graph comprises calculating the number of bends in each graph.

41. (New) The method of claim 40, wherein the bends are diagonal bends.

42. (New) The method of claim 36, wherein the partitioning grid having a plurality of edges between said slots, wherein computing multiple attributes of each

connection graph comprises identifying the edges intersected by each graph.

43. (New) The method of claim 42, wherein said partitioning grid having a particular structure, wherein said edges are defined based on a wiring model for the IC layout and on the structure of the partitioning grid.

44. (New) The method of claim 36, wherein the partitioning grid having a plurality of interconnect-line paths between said slots, wherein computing multiple attributes of each connection graph comprises identifying the paths used by each graph.

45. (New) The method of claim 44, wherein said partitioning grid having a particular structure, wherein said interconnect-line paths are defined based on a wiring model for the IC layout and on the structure of the partitioning grid.

46. (New) The method of claim 36, wherein the partitioning grid having a plurality of interconnect-line paths between said slots, wherein computing multiple attributes of each connection graph comprises calculating the length of each graph and identifying the paths used by each graph.

47. (New) The method of claim 36, wherein the partitioning grid having a plurality of edges between said slots, wherein computing multiple attributes of each connection graph comprises calculating the length of each graph and identifying the edges intersected by each graph.

48. (New) The method of claim 36, wherein the partitioning grid is formed by

a set of partitioning lines.

49. (New) The method of claim 48, wherein the partitioning lines are horizontal and vertical lines.

50. (New) For an electronic design automation ("EDA") application that performs placement operations, a method of pre-computing costs of placing circuit elements within an integrated-circuit ("IC") layout, the method comprising:

a) defining a partitioning grid having a plurality of slots, said partitioning grid for partitioning, during a placement operation, a region of an IC layout into a plurality of sub-regions corresponding to said slots;

b) for each combination of said slots, identifying at least one connection graph that models the topology of interconnect lines necessary for connecting the combination of said slots;

c) computing the length and number of bends in each of said connection graphs;

d) for each particular combination of said slots, storing the length of a connection graph identified for that particular combination of said slots, wherein when more than one connection graphs are defined for that particular combination of said slots, the method storing the length of shortest connection graph that has less than a predetermined number of bends.

51. (New) The method of claim 50 further comprising:

for each particular combination of said slots that has more than one identified connection graphs, storing the length of shortest connection graph that has less than a second predetermined number of bends, when none of the connection graphs for the particular combination of said slots have less than the first predetermined number of bends.

52. (New) A method of placing circuit modules in a region of an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements, wherein a plurality of nets represent interconnections between said circuit elements, each net defined to include a set of circuit elements, the method comprising:

a) partitioning the IC region into several sub-regions;

b) selecting a net;

c) identifying the set of sub-regions containing the circuit elements of the selected net,

d) retrieving from a storage structure multiple pre-computed attributes of a set of one or more interconnect lines necessary for connecting the identified set of sub-regions;

e) computing a placement cost of said net within said region by using the retrieved attributes.

53. (New) The method of claim 52 further comprising:

a) changing the position of a circuit element of the net from one sub-region to another;

b) identifying a new set of sub-regions that contain the circuit elements of the net;

c) retrieving multiple pre-computed attributes of a different set of interconnect lines necessary for connecting the identified new set of sub-regions;

d) computing a new placement cost of said net within said region by using the attributes retrieved for the different set of interconnect lines.

54. (New) A method of placing circuit modules in a region of an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements, wherein a plurality of nets represent interconnections between said circuit elements, each net defined to include a set of circuit elements, the method comprising:

a) partitioning the IC-layout region into several sub-regions;

b) for each particular net, identifying the set of sub-regions containing the circuit elements of the particular net,

c) for each particular net, retrieving multiple pre-computed attributes of a connection graph that models the topology of interconnect lines needed to connect

the identified set of sub-regions of the particular net;

d) computing a placement cost for the IC layout within said region by using the retrieved attributes.

55. (New) The method of claim 54, wherein the connection graphs are Steiner trees.

56. (New) The method of claim 54, wherein the connection graphs are minimum spanning trees.

REMARKS

This Preliminary Amendment is concurrently filed with the above-entitled application, which is a continuation application of a presently pending application entitled "Recursive Partitioning Placement Method and Apparatus," filed on December 6, 2000. In this Preliminary Amendment, Applicants have changed the title of this application,

inserted a reference to the related parent application, canceled claims 1-27, and added claims 28-56. Accordingly, claims 28-56 are currently pending in this application.

Respectfully submitted,

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Dated: December 15, 2000

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